

## METHOD FOR MAKING A WAFER-PAIR HAVING SEALED CHAMBERS

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### BACKGROUND

The present invention pertains to vacuum encapsulated microstructure devices. It particularly pertains to the vacuum seal of a cavity between two wafers, and more particularly to the fabrication of such two wafers having a pluggable hole for evacuation of gases from the cavity.

Various devices, such as microstructure infrared (IR) devices, require vacuum encapsulation for optimal performance. Conventional vacuum packaging is complex and costly. Known prior art approaches to wafer level vacuum sealing cannot yield adequately low pressures, the best in the range of 0.5 torr. Such pressures resulted in 50 percent signal losses for thermoelectric (TE) devices as an example.

### SUMMARY OF THE INVENTION

The present invention involves the sealing of two wafers together resulting in a cavity between the wafers with a pluggable hole for the evacuating of gases from the cavity. The hole, after evacuation of gases from the cavity, is plugged with deposited metal. The result is an integral vacuum package (IVP). This approach permits the sealing of the two wafers together without having to create the vacuum seal at the same time. The final vacuum seal can be done in a high vacuum by either evaporation or the sputtering of a thick layer of metal to plug the small pump-out port. This approach allows a thorough baking out of the wafer to wafer seals and interior surfaces prior to a final vacuum seal. It separates the two functions and does not limit the bake-out to the solder processing steps. There is independent control over sealing and bake-out to maximize bond yield and minimize residual pressure. This approach also permits clear access of each vacuum cavity directly, thereby avoiding the need to pump from the periphery of the wafer inwards. The procedure here has been implemented and resulted in vacuum levels below 10 millitorr of residual pressure as measured by pressure sensors within the cavity. The seals cover significant substrate topography. Seals over topography of 0.25 microns have been demonstrated. The required processing temperatures are below 300 degrees Centigrade (C.). These chips can be handled with conventional chip handling equipment. Yields for this process exceed 90 percent. Costs of the present vacuum-sealed chips are 80 to 90 percent less than that of conventionally vacuum-sealed chips. The present approach results in sealed devices that have high temperature longevity for pressures below 100 millitorr; ten years is indicated by test data for ambient temperatures up to 150 degrees C. Each cavity may have a gas instead of a vacuum. Each cavity, chamber or volume may contain detectors such as thermoelectric detectors, devices, bolometers, or may contain emitters.

### BRIEF DESCRIPTION OF THE DRAWING

FIGS. 1a and 1b show plan and cutaway side views of a detector chip having a chamber with a deposited plug vacuum seal.

FIG. 2 shows a perspective view of the device chip having the deposited plug vacuum seal.

FIG. 3 reveals a wafer having a plurality of detectors with a deposited vacuum seal on a plurality of plugs.

FIGS. 4a, 4b, 4c, 4d, 4e, 4f, 4g, 4h, 4i, 4j, 4k, 4l and 4m illustrate the fabrication process for a detector wafer.

FIGS. 5a, 5b, 5c, 5d, 5e and 5f illustrate the fabrication process for a top cap wafer.

FIGS. 6a, 6b and 6c illustrate the steps of aligning, bonding and sealing the detector and top cap wafers.

### DESCRIPTION OF THE EMBODIMENT

FIGS. 1a, 1b and 2 show an illustration of a device 10 having a vacuum pump-out port 11 and a deposited plug final vacuum seal 12. The deposited layer 12 seals port 11 to hermetically seal chamber 16. Wafers 13 and 14 are of the same material, such as silicon, thereby having the same coefficients of thermal expansion. Wafers 13 and 14 are adhered together at a solder seal ring 15. Wafer 13 is the detector chip and wafer 14 is the top cap. Cavity 16 is the chamber that contains an array 17 of detectors on the surface of wafer 13 and detects radiation which may come through an anti-reflective coated silicon window of top cap 14.

Cavity 16 is effected by a recess of about 125 microns into wafer 14 having a border 18. It is this cavity that is outgassed to result in a cavity vacuum. Top cap 14 is about 430 microns thick and chip 13 is about 500 microns thick. Seal ring 15 is a composition of 90 percent lead and 10 percent indium. Plug 12 is about 20 microns thick and is a composition of 50 percent lead and 50 percent indium.

FIG. 3 shows a wafer 20 having multiple chips 10 having a wafer-to-wafer sealing of the same material for multiple cavities. Cavities 16 can be baked out and outgassed since each chamber 16 has an open port 11. Then in an environment of a vacuum, a deposition of metal 12 is applied to the wafer 13 surface having ports 11 and thereby close ports 11 and seal chambers 16 closed with a vacuum in the chambers. Solder balls for sealing of the ports closed has been tried with little success of maintaining a vacuum or low pressure in the cavities. The present wafers 13 and 14, after bonding and sealing, may be sawed into individual chips without breakage since the sealed top cap protects the fragile microstructure devices 17. Further, the plug will not be disturbed since it is a deposited layer 12 rather than some dislodgable solder ball or plug.

A process for developing chip 10 is shown in FIGS. 4a through 4m. The process for detector wafer 13 starts out with a double polished silicon wafer 13. In FIG. 4a, one micron layers 22a and 23a of thermal SiO<sub>2</sub> are grown on wafer 13, and 0.3 micron layers 22b and 23b of low pressure chemical vapor deposited (LPCVD) Si<sub>3</sub>N<sub>4</sub>. Si<sub>3</sub>N<sub>4</sub> layer 22b and SiO<sub>2</sub> layer 22a are removed from the "front" of wafer 13. A 1000 angstroms of a thermal SiO<sub>2</sub> layer 24 is grown on the front of wafer 13 in FIG. 4b. A layer 25 of 2000 angstroms of Si<sub>3</sub>N<sub>4</sub> (bottom bridge nitride) is deposited on layer 24 in FIG. 4c. The first metal NiFe (60:40) of a thermocouple is deposited as a 1100 angstrom layer 26 on layer 25 and then first metal layer 26 is patterned with a first mask by ion milling resulting in the layout of FIG. 4d.

For the second metal of the thermocouple detectors, a thousand angstrom layer 27 of chromium is deposited on layers 25 and 26. Layer 27 in FIG. 4e is patterned with a second mask by ion milling and wet etching. A layer 28 consisting of 6000 angstroms of Si<sub>3</sub>N<sub>4</sub> is deposited on metal layers 26 and 27, and layer 25, as the top bridge nitride in FIG. 4f. An absorber 29 is deposited on layer 28 of FIG. 4g and patterned with a third mask. Absorber 29 is capped with a layer 30 of Si<sub>3</sub>N<sub>4</sub>. Plasma etched vias 31 to metal layer 27 are patterned and cut with the use of a fourth mask, as shown in FIG. 4h. Plasma etched vias 32 in FIG. 4i for the final etch